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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WILLIAMS, LAWRENCE B	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/827,273	SCHLANGER ET AL.	
	Examiner	Art Unit	
	Lawrence B Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-30* is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because: Examiner suggests applicant label the drawing in Fig. 3 as (a), (b) (c), (d) as done in Fig. 4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: Examiner suggests that applicant include references to all figures included in Figs 3, and 4.

Appropriate correction is required.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has submitted an incomplete claim. Line 13 of the claim on page 19 reads as follows: "...levels is the same or different than the logic levels of the respective ones of said...".

Accordingly, the claim has not been further treated on the merits.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-20, 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mos et al. (US Patent 6,260,146 B1) in view of Lombreschi (US Patent 5,818,274).

(1) With regard to claim 1, Mos et al. discloses in Fig. 4, and a digital processor, said digital processor (404) having an input coupled to the output coupled with a leading edge apparatus comprising a zero crossing detector, whereby said digital processor periodically reads said logic state and stores the logic level thereof, wherein said digital processor compares the logic level of a subsequently read logic state with the stored logic level so as to determine whether the stored logic level is the same or different than the logic level of said subsequently read logic state, if different then an event has occurred and if the same then no event has occurred (col. 8, lines 19-col. 8, lines 52).

Mos et al. does not however disclose a bistable memory device, said bistable memory device having an input adapted for detecting the occurrence of an event and an output representing a logic state of said bistable memory device, wherein said logic state is at either a first or a second logic level such that the logic level of said logic state changes each time the event is detected.

However, Lombreschi et al. discloses in Fig. 5, a bistable memory device (FFSR), said bistable memory device having an input adapted for detecting the occurrence of an event and an output representing a logic state of said bistable memory device, wherein said logic state is at either a first or a second logic level such that the logic level of said logic state changes each time the event is detected (abstract).

One skilled in the art would have clearly recognized a bistable memory device (FFSR), said bistable memory device having an input adapted for detecting the occurrence of an event and an output representing a logic state of said bistable memory device, wherein said logic state is at either a first or a second logic level such that the logic level of said logic state changes each

time the event is detected. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Lombreschi et al. to modify the invention of Mos et al. to as a known and practical method of detecting logic levels (col. 1, lines12-18; col. 2, lines 22-27).

(2) With regard to claim 2, Lombreschi et al. also discloses in Fig. 5, wherein the bistable device is a flipflop.

(3) With regard to claim 3, Lombreschi et al. also discloses wherein the flip-flop is selected from the group consisting of D, J-K, R-S and toggle flip-flops (col. 1, lines 25-32).

(4) With regard to claim 4, though neither Mos et al. nor Lombreschi et al. disclose the bistable memory device is a counter, it is well known in the art that counters, latches, flip-flops can used to perform similar functions. It is also known in the art that a counter comprises a series of flip-flops. Therefore it would be simply a design choice as to what device one would incorporate which would not constitute an inventive step.

(5) With regard to claim 5, claim 5 inherits all limitations of claim 4, above. Furthermore, it would be obvious to choose a counter from the group consisting of an asynchronous and a synchronous since these the most commonly known.

(6) With regard to claim 6, though neither Mos et al. nor Lombreschi et al. disclose the bistable memory device is a latch, it is well known in the art that counters, latches, flip-flops can used to perform similar functions. Therefore it would be simply a design choice as to what device one would incorporate which would not constitute an inventive step.

(7) With regard to claim 7, Mos et al. also discloses wherein said digital processor is selected from the group consisting of a microcontroller, a microprocessor, a programmable logic array and a application specific integrated circuit (col. 8, lines 17-18).

(8) With regard to claim 8, Mos et al. also discloses wherein said digital processor comprises a central processing unit (col. 8, lines 17-39), a random access memory (410) and a read only memory (col. 8, lines 43-46).

(9) With regard to claim 9, Mos et al. also disclose in Fig. 4, wherein the digital processor comprises a bistable memory device (406, 412) and logic gates (col. 8, lines 53-56).

(10) With regard to claim 10, Mos et al. also disclose wherein said logic gates are selected from the group consisting of inverter, OR, NOR, AND, NAND, XOR, XNOR (col. 8, lines 53-56).

(11) With regard to claim 11, Mos et al. also discloses in Fig. 7, the apparatus further comprising plurality of bistable memory devices (405, 407) for detecting a plurality of events, wherein said plurality of bistable memory devices are coupled to said digital processor (419).

(12) With regard to claim 12, claim 12 inherits all limitations of claim 1, above as claim 12 discloses the method of used by the apparatus of claim 1.

(13) With regard to claim 13, Lombreschi et al. also discloses in Fig. 5, wherein the bistable device is a flipflop.

(14) With regard to claim 14, Lombreschi et al. also discloses wherein the flip-flop is selected from the group consisting of D, J-K, R-S and toggle flip-flops (col. 1, lines 25-32).

(15) With regard to claim 15 though neither Mos et al. nor Lombreschi et al. disclose the bistable memory device is a counter, it is well known in the art that counters, latches, flip-flops

can used to perform similar functions. It is also known in the art that a counter comprises a series of flip-flops. Therefore it would be simply a design choice as to what device one would incorporate which would not constitute an inventive step.

(16) With regard to claim 16, claim 16 inherits all limitations of claim 15, above. Furthermore, it would be obvious to choose a counter from the group consisting of an asynchronous and a synchronous since these the most commonly known.

(17) With regard to claim 17, though neither Mos et al. nor Lombreschi et al. disclose the bistable memory device is a latch, it is well known in the art that counters, latches, flip-flops can used to perform similar functions. Therefore it would be simply a design choice as to what device one would incorporate which would not constitute an inventive step.

(18) With regard to claim 18, Mos et al. also discloses wherein said digital processor is selected from the group consisting of a microcontroller, a microprocessor, a programmable logic array and a application specific integrated circuit (col. 8, lines 17-18).

(19) With regard to claim 19, Mos et al. also discloses wherein said digital processor comprises a central processing unit (col. 8, lines 17-39), a random access memory (410) and a read only memory (col. 8, lines 43-46).

(20) With regard to claim 20, Mos et al. also disclose in Fig. 4, wherein the digital processor comprises a bistable memory device (406, 412) and logic gates (col. 8, lines 53-56).

(21) With regard to claim 22, Lombreschi et al. discloses where the first logic level is a logic low and the second logic level is a logic high (col. 1, lines 19-25).

(22) With regard to claim 23, Lombreschi et al. also discloses where the first logic level is a logic high and the second logic level is a logic low (col. 1, lines 19-25).

(23) With regard to claim 24, Mos et al. also discloses a logic circuit for producing a clock pulse each time a transition from a low to a high or a high to a low logic level is detected (col. 8, lines 53-65).

(25) With regard to claim 25, Lombreschi et al. also discloses in Fig. 1, a logic circuit for producing a clock pulse each time a transition from a low to a high or a high to a low logic level is detected wherein said logic circuit is connected between the event and the input of said bistable device (col. 1, lines 33-46).

(26) With regard to claim 26, though Lombreschi et al. does not disclose the logic circuit comprising an XOR and an even number of inverters, such a circuit would be mere design choice with the use of digital logic to implement the same function as the invention of Lombreschi et al.

Allowable Subject Matter

8. Claims 27-30 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter: The instant application discloses a bistable memory device and digital processor for event detection. A search of prior art records has fail to disclose a bistable memory device and digital processor for event detection comprising; "a second bistable memory device, said bistable memory device having an input adapted for detecting the occurrence of an event and an output representing a logic state of said bistable memory device, wherein said logic state is at either a first or a second logic level such that the logic level of said logic state changes each time the event is detected; and a digital processor, said digital processor having an input coupled to the output of said first bistable memory device and another input coupled to the output of said

second bistable memory device, whereby said digital processor periodically reads said logic states and stores the logic levels thereof wherein said digital processor compares the logic level of a subsequently read logic state with the stored logic level so as to determine whether the stored logic level is the same or different than the logic level of said subsequently read logic state, if different then an event has occurred and if the same then no event has occurred; wherein said event detector is coupled between said transmitter said computer, and said receiver and said computer such that said first bistable memory device is coupled to said receiver and said second bistable memory device is coupled to a serial output of said computer" as disclosed in claim 27.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.) Kweon discloses in US Patent 5,438,328 a Circuit For Measuring Pulse Width Of Remote Control Signal.

b.) Kirkpatrick discloses in US 4,740,891 an Asynchronous State Machine.

c.) Dorweiler et al. discloses in US Patent 6,075,385 an Intelligent Precharger For A Dynamic Bus.

d.) Lin discloses in US Patent 4,940,904 an Output Circuit For Producing Positive And Negative Pulses At A Single Output Terminal.

e.) Earnest discloses in US Patent 5,982,837 an Automatic Baud Rate Detector.

f.) D'Orazio et al. discloses in US Patent 3,898,689 a Code Converter.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
November 30, 2004

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